ABSTRACT

A method and apparatus for delivering APIC interrupts to a processor, and between processors, as FSB transactions. Interrupts and hardware signals, generated by a PCI device, are converted into an upstream memory write interrupt and further converted into an FSB interrupt transaction, received by a processor. Interrupts marked as lowest priority re-directable are redirected based on task priority information. Support for XTPR transactions to update XTPR registers is provided. Preferred ordering of XTPR update transactions and interrupts to be redirected is provided.